SGT1 STE Bus Compatible Graphics and Text Terminal

Hardware Manual

Board One

Contents

Section 1. Introduction

The SGT1 is a graphics terminal system interfaced to the STEbus. The full system consists of a two board set, but the base board can provide powerful facilities on its own. It contains the bus interface, onboard 6803E processor, 64K bytes of memory, graphics controller and basic display multiplexing. On its own, this board can provide two graphics modes, with output to a standard TTL RGB monitor. The second board contains further display multiplexing and analogue circuitry to provide 2 modes with analogue RGB output, a high-resolution monochrome output and a genlock input to synchronise the boards to an external video source. Firmware is supplied as standard with the system, but this manual is intended to explain enough of the hardware to enable users to modify or create special-purpose software for their individual needs if necessary (please see software manual).

Section 2. Typical Applications

- Graphics terminal emulation
- Video presentation
- Video titling and computer graphics effects
- Circuit design and layout
- Process control information display
- Visualisation of complex concepts

Section 3. Circuit Description

The heart of the system is the finite state machine formed by IC27 (a 32 x 8 PROM) and IC31 (an octal latch). This is driven either by the 26.75 MHz delay line oscillator on Board One, or by Board Two's oscillator in genlock mode, and provides all the main timing for both the boards.

The 6845 graphics controller chip, IC17, shares access for the 64K of DRAM with the 6803E CPU, IC14, through multiplexers IC19, IC20, IC23 and IC24. The order of access for the two devices is 6845 Row, 6845 Column, 6803E Row, 6803E Column, 6845 Row .... etc. The timing for this is possible because the 6803E CPU has externally driven E and AS lines, and this enables its synchronisation with the rest of the system.

IC11 is a 28-pin socket capable of holding up to 16K of EPROM, which holds the system's firmware. It is mapped into the memory map a block of 8K, with the upper and lower 8K sections being selected by the PROMBANK signal from IC14 Port 1 Bit 3. Since the 6803E has an address/data bus in which the lower byte of the address and the data byte are multiplexed, IC8 (an octal latch), driven by IC31, is used to separate them.

The memory map decoding is handled by IC7, a custom PAL, which decodes memory as shown on in Section 7 (page 9). The bus interface is organised and timed by another custom PAL, IC5. IC3 buffers the miscellaneous STE control lines to the PAL, and IC2 decodes the top eight I/O address lines, sending the /ADDE input to the PAL active when they correspond to the address set by the jumpers in LK1. When a valid bus access is recognised by the PAL, it determines whether it is at (BASE ADDRESS), or (BASE ADDRESS+1). If it is at the latter then it is a status read, so the PAL enables half of IC6 - which puts the four status signals BUSY, ERROR, DREADY and ACTIVE onto the lower nibble of the bus - and sends a DTACK* back to the STEbus via TR1, without bothering the 6803.

Section 3. Circuit Description

If the access is at the board's base address, it is a data read or write, and so the PAL behaves as follows:-

If /ACTIVE is high, it sends back a DTACK* immediately, since this indicates that the CPU is not in a fit state to process the access (it might, for example, have just been reset and be still sorting itself out internally).

Otherwise, if /ACTIVE is low and /BUSY is low the PAL activates IC1 if this is a write to the board, and sends an /NMI to the 6803E which stores the incoming byte (write), or places a byte in IC4 (read), modifies the status bits as necessary, then tells the PAL it has finished by setting /BUSY high.

IC1 buffers SYSCLK, which is used to clock the PAL, and SYSRST* which controls IC10, a reset-generating chip. The type of the last access (read or write) is held on IC5 pin 13, which is connected to IC14 pin 14 (P11).

At the output end, IC30 latches data out, a byte at a time, to IC33, which outputs the top and bottom nibbles of this byte alternately at twice the speed. At this stage of multiplexing, the bus goes off to the second board, but to enable the base board to be used alone, another custom PAL combines these lines with various clocks, processor control lines and the display timing output from the 6845 to produce either a 320 x 288 pixel 8-colour, or a 640 x 288 pixel 4-colour display on a standard TTL RGB monitor.

Section 4. Specification

Temperature range	- 0C to 50C	
Power consumption	- < 1.25A (Typ.)	
Line period	- 64 us	
Frame period	- 20 ms	
Line blanking	- 12 us	
Frame blanking	- 24 lines	
Video bandwidth	Mode 4:	- 6.2 MHz
	Mode 2:	- 12.3 MHz
	Mode 1:	- 24.6 MHz
Onboard RAM	61440 bytes accessible in total	
Onboard EPROM	Socket for up to 16K bytes	

Section 5. Links and Options

Note: an asterisk (*) indicates the standard link connection, as supplied.

The boards are described as if you were viewing them from the component side with PL4 to the right.

STEbus address: LK1

This determines the address of the data port of the SGT1 on the STEbus. The address of the status port is one above this. The standard base address of the board is 144 (decimal).

LK1

```
     o H o          - A4
*    o G o          - A5
*    o F o          - A6
     o E o          - A7
     o D o D o   *  - A8
     o C o C o   *  - A9
     o B o B o   *  - A10
     o A o A o   *  - A11

     1   2
```

Making a link in column 1 means that that address line is low. Leaving the link out means that it is high when the board is being addressed.
Making a column 2 link causes that address line to be ignored in the address comparison.

CPU type: LK2

LK2

```
o A o
```

This link must be left open.

Genlock operation: LK3

LK3

```
*    o A o B o
```

Make only link A for normal operation using the Board 1 oscillator.
Make only link B if running ' genlocked ' to an external video source via Board 2.

Section 6. Connections

STEBus connections

PL1: STE bus 64-way a/c DIN41612

		Row a	Row c
pin	32	gnd	gnd
	31	+5v	+5v
	30	-12v	+12v
	29	SYSCLK	+VSTBY
	28	BUSAK0*	BUSAK1*
	27	BUSRQ0*	BUSRQ1*
	26	gnd	ATNRQ7*
	25	ATNRQ6*	ATNRQ5*
	24	ATNRQ4*	ATNRQ3*
	23	ATNRQ2*	ATNRQ1*
	22	ATNRQ0*	SYSRS7*
	21	TRFERR*	gnd
	20	DATACK*	DATSTB*
	19	ADRSTB*	gnd
	18	CM2	CM1
	17	CM0	A19
	16	A18	A17
	15	A16	A15
	14	A14	A13
	13	A12	A11
	12	A10	A9
	11	A8	A7
	10	A6	A5
	9	A4	A3
	8	A2	A1
	7	A0	gnd
	6	D6	D7
	5	D4	D5
	4	D2	D3
	3	D0	D1
	2	+5v	+5v
	1	gnd	gnd

Section 6. Connections

PL2: Serial connector

1	GND
2	SERCLK IN
3	RDATA
4	TDATA

PL3: Light pen connector

1	LPEN IN
2	GND

PL4: Inter-board connector

64-way Berg connector

	1	CD0	VSYNC	2	
	3	CD1	CD2	4	
	5	CD3	GREEN	6	!!
!!	7	RED	CSYNC	8	!!
!!	9	BLUE	HSYNC	10	
	11	MV1	MV0	12	
!!	13	0V	MV2	14	
	15	+5V	+5V	16	
	17	MODSEL1	MV3	18	
	19	CV2	MODESEL2	20	
	21	/CV3	DISPEN	22	
	23	/MWR	/SCLK	24	
	25	+5V	+5V	26	
	27	0V	0V	28	
	29	VL4	VL5	30	
	31	VL1	VL0	32	
	33	VL6	VL7	34	
	35	VL3	CV1	36	
	37	SYNCLK	VL2	38	
	39	VLOCK	E	40	
	41	0V	0V	42	
	43	+5V	+5V	44	
	45	0V	/VCYC	46	
	47	0V	0V	48	
	49	CA3	CA2	50	
	51	CA1	CA0	52	
	53	0V	CLK	54	
	55	0V	CHARCLK	56	
	57	0V	AS	58	
	59	0V	ADDSEL	60	
	61	+5V	+5V	62	
	63	+12V	-12V	64	

All pins on the connector are outputs except for pin 37, which is the clock output from the genlock circuit on Board 2.
Pins marked '!!' are not used by Board Two, and are the RGB monitor connections.

Section 7. Using the board

The mapping of both internal and external devices within the 64K map of the 6803E is shown below:

Address (hex)	Device
0000	6803E Port 1 Data Direction Register (1=O/P,0=I/P)
0001	6803E Port 2 D.D.R.
0002	6803E Port 1 Data Register
0003	6803E Port 2 D.R.
0004 to 0007	Not used
0008	6803E Timer control and Status Register
0009	6803E Counter (High Byte)
000A	6803E Counter (Low Byte)
000B	6803E Output Compare Register (High Byte)
000C	6803E O.C.R. (Low byte)
000D	6803E Input Capture Register (High byte)
000E	6803E I.C.R. (Low byte)
000F	Not used
0010	6803E Rate and Mode Control Register
0011	6803E Transmit/Receive Control and Status Register
0012	6803E Receive Data Register
0013	6803E Transmit Data Register
0014	6803E RAM Control Register
0015 to 03FF	Not used
0400	6845 Register Select
0401	6845 Data Register
0402 to 07FF	Not used
0800	STEbus Output Latch (WR) or Input Port (RD)
0C00 to 0C0F	Board 2 colour mapping RAM (WO)
0C10 to 0FFF	Not used
1000 to DFFF	RAM (shared by the 6803E and 6845)
E000 to FFFF	If MAP (6803E Port 1 Bit 0) is high, this is EPROM (if 16K EPROM, the high and low 8K segments are selected by PROMBANK : 6803E Port 1 Bit 3) If MAP is low, this is the top 8K of RAM

Section 7. Using the board

Use of the 2 ports on the 6803E is described below:

PORT 1 (8 bits)

Bit 0 (pin 13) - Output - MAP. Controls top 8K of memory. High to map EPROM in, low to map in RAM.

Bit 1 (pin 14) - Input - TYPE. High if last STEbus data port access was a read, low if it was a write.

Bit 2 (pin 15) - Output - /BUSY. Informs STEbus PAL of current state of 6803. Also present on Bit 3 of the STEbus status port.

Bit 3 (pin 16) - Output - PROMBANK. Selects which half of a 16K EPROM is used. High for top half, low for lower half. Defaults to upper half on RESET. Has no function when using an 8K EPROM.

Bit 4 (pin 17) - Output - ADDSEL. Goes to Board 2. Put low before changing the colour palette, high for normal operation.

Bit 5 (pin 18) - Output - MODESEL2. Goes to Board 2, where it selects the palette currently in use.

Bit 6 (pin 19) - Output - MODESEL1. Goes to the output PALs on both boards. Selects the display mode. High for Mode 4, low for Modes 2 and 1.

Bit 7 (pin 20) - Output - /ERROR. Goes to STEbus status port Bit 2. Low to indicate that an ERROR has occured.

PORT 2 (5 bits)

Bit 0 (pin 8) - Output - /ACTIVE. When high, tells IC5 to mask /NMI. In this condition, bus accesses are suspended until /ACTIVE goes low again. This signal appears on Bit 0 of the status port.

Bit 1 (pin 9) - Reserved

Bit 2 (pin 10) - Output - /DREADY. Determines Bit 1 of the status port.
If configured as an input then /DREADY is not available on the bus but this pin can be used as BCK input. This pin goes to PL2 pin 2.

Bit 3 (pin 11) - Input - RDATA. Intended for use as a serial data input, this pin goes to PL2 pin 3.

Bit 4 (pin 12) - Output - TDATA. Intended for use as a serial data output, this pin goes to PL2 pin 4.

6845 CRTC Register Details.

To access a 6845 register, the register number (0 to 17d) is written to 0400h. The data can then be read from or written to this register at 0401h. Details of the registers are shown below:

Register	Read or write	Function	Normal value
00 (bits 0-4)	WO	Total number of columns	224 d
01	WO	Number of columns displayed	160 d
02	WO	Horizontal Sync. Position (can shift picture to left or right)	181 d
03 (bits 0-3)	WO	Horizontal Sync. Pulse Width	(15 +
(bits 4-7)	WO	Vertical Sync. Pulse Width	64 =) 79 d
04 (bits 0-6)	WO	Total number of rows	40 d
05 (bits 0-4)	WO	Number of additional rasters per screen	8 d
06 (bits 0-6)	WO	Number of rows displayed	34 d
07 (bits 0-6)	WO	Vertical Sync. Position (can shift picture up or down)	37 d
08 (bits 0-1)	WO	0=Non-interlace mode 1=Non-interlace mode 2=Interlace Sync mode 3=Interlace Sync and Video mode	(0 +
(bits 4-5)	WO	0=No skew on DISPTMG 1=1 column skew on DISPTMG 2=2 column skew on DISPTMG 3=No video output	16=) 16 d
09 (bits 0-4)	WO	Number of rasters in a character	7 d
0A		Not used	-
0B		Not used	-
0C (bits 0-5)	RW	Display start address (High byte)	1 d
0D	RW	Display start address (Low byte)	0 d
0E	RW	Cursor address (High byte)	1 d
0F	RW	Cursor address (Low byte)	0 d
10	RO	Light pen position (High byte)	? d
11	RO	Light pen position (Low byte)	? d

When running in the genlock mode of operation, register 5 must be reset to zero, so that vertical scan time becomes short enough for the SGT1 to reach the end of its vertical scan just before the video source that it is to synchronise with.

The light pen registers return a value proportional to the number of rasters that are output between the start of a vertical scan, and the light pen input going high. A constant will have to be subtracted from this value to account for variations in the speed of the phosphor of the C.R.T., rise-time of the light pen, etc.

Section 7. Using the board

Interrupts

The 6803E /NMI line is taken from the PAL controlling the STEbus, and is asserted when a read or write of the SGT1 is attempted by another CPU. It is masked when ACTIVE (6803E Port 2 Bit 0) is high, and vectors through FFFC (MSB) and FFFD (LSB).

The 6803E /INT line is asserted at the beginning of every frame, and can be used for updating the colour palette, moving sprites, keeping a real-time clock, and activating other processes that are time-dependent or that may cause glitches on the display. It vectors through FFF8 (MSB) and FFF9 (LSB).

Other interrupts and their vectors are shown below:

MSB	LSB	Interrupt
FFFE	FFFF	RESET
FFFA	FFFB	Software Interrupt
FFF6	FFF7	Input Capture
FFF4	FFF5	Output Compare
FFF2	FFF3	Timer Overflow
FFF0	FFF1	Serial Interrupt

If it is intended to modify the firmware supplied with the SGT1, it is strongly advised that the MC6803E Data sheet be obtained from your Motorola (R) distributor.

Board 1 can be used alone to drive a standard TTL-compatible RGB monitor. In this case connect the monitor signals (R,G,B,COMPSYNC,GND) to PL4 (as shown in Section 6). NOTE: As supplied, Board One produces a negative composite sync output (as standard on the majority of modern monitors made by, for example, Microvitec (R)).

International Video Standards

In countries using a different video standard to the U.K., it is usually possible to modify the board to work with these standards by simply re-programming the 6845 registers. For example, in the U.S.A. the line period is the same, but the frame period is shorter, and this can be accomodated by changing the Vertical Total register. In countries where the line period is considerably different to the U.K., it will probably still be possible to sync. with a monitor, but the picture may be the wrong size. If this is unacceptable (e.g. the monitor cannot be re-adjusted sufficiently to accommodate the change), then DL1 may have to be changed. Contact Arcom for further details.

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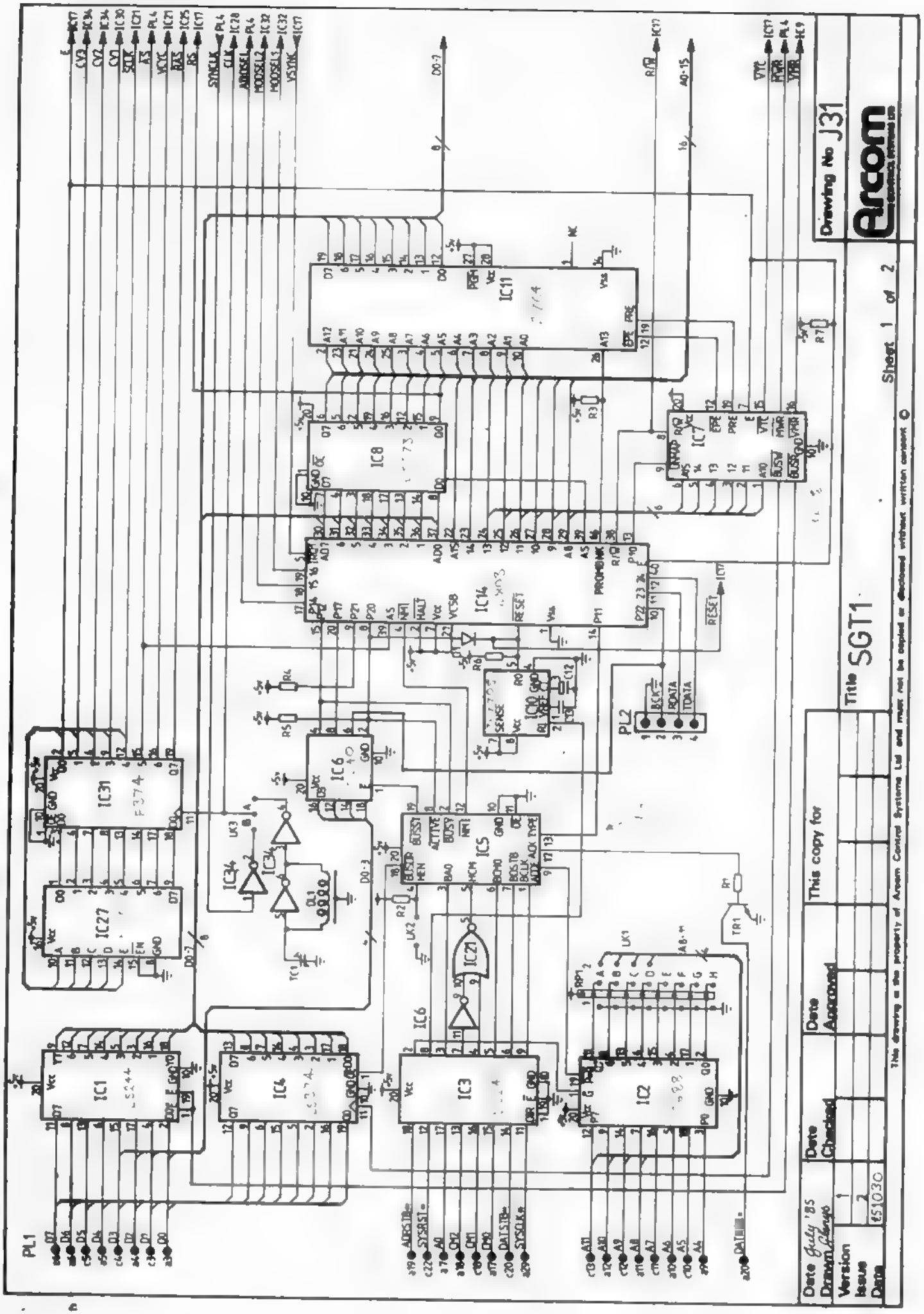
Section 8. Fault Finding Guide

All Arcom boards are thoroughly inspected and soak-tested before despatch, and so the likelihood of a board being faulty on arrival is small.
If the board has never worked, it is possible that it was damaged in transit, so please inspect it carefully for physical damage before proceeding with this guide.

Fault	Cause	Remedy
No picture	No power	Check power to SGT1 and monitor
	Faulty connector(s)	Check that the RGB signals are reaching the monitor.
	Blank screen	Are you sure that you have sent the right bytes ?
Accesses to the board 'hang'	Wrong address Faulty bus/socket	Check that the address that you are using corresponds to the jumpers in LK1
Picture too large	Incorrect SGT1 clock frequency or maladjusted monitor	Trimmer capacitor TC1 can be adjusted (using a tuning tool) until the picture is the correct size, if the monitor has no controls to adjust its screen width
	Wrong T.V. standard	Is your local T.V. standard compatible with the U.K. standard ?
Jumping picture	Bad sync(s)	Check that you are supplying your monitor with all the syncs it needs, and that they are of the correct polarity. Check that they are reaching the monitor.
	Wrong frequency	Check that the monitor that you are using is set up to work with standard U.K. line and frame rates.
'Wavy' picture	External E.M.I.	Is the SGT1 close to any sources of strong electro-magnetic interference (for example the monitor or a switched-mode power supply)? Try moving any possible sources away or shielding the board better.
Skewed picture	Bad ground	A skewed picture is usually the result of an insufficient ground between the output device and the monitor. Check that you have connected the ground from SGT1 PL4 pin 8 to your monitor input ground (this is not necessarily the same ground as the monitor's case).
	Frequency mis-match	Check that your monitor is working at the correct frequency.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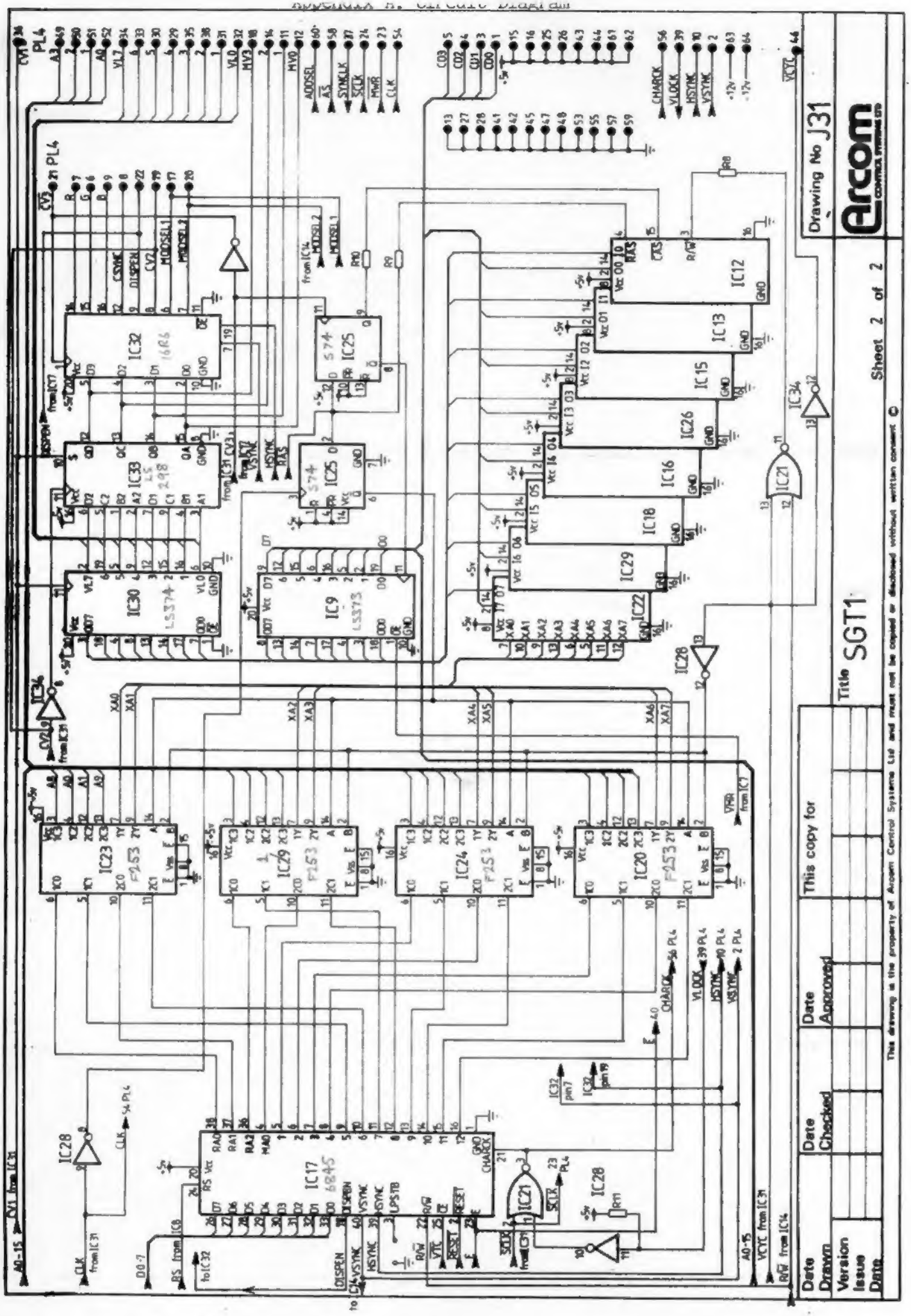
Arcom
Title SGT1
Sheet 1 of 2
This copy for
Date Assessed
Date Checked
Date July '85
Drawn
Version 1
Issue 2
Date 851030
IC11
IC8
IC7
IC14
IC10
IC31
IC27
IC6
IC5
IC4
IC1
IC3
IC2
PL1
PL2
RESET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Arcom
Sheet 2 of 2
Title SGT1
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Date Approved
Date Checked
Date Drawn
Version
Issue
Date
This drawing is the property of Arcom Control Systems Ltd and must not be copied or disclosed without written consent ©
IC12
IC13
IC15
IC26
IC16
IC18
IC29
IC22
IC34
IC21
IC28
IC32
IC30
IC9
IC25
IC33
IC23
IC24
IC20
IC17
IC28

Appendix B. Component Identification

SEMICONDUCTORS

IC1	74LS244
IC2	74LS688
IC3	74LS245
IC4,30	74LS374
IC5,32	PAL16R6
IC6	74 F240
IC7	PAL16L8
IC8,9	74LS373
IC10	TL7705A
IC11	2764 Firmware EPROM
IC12,13,15,16 18,22,26,29	4164-3
IC14	6803-EL
IC17	6845-SP 5
IC19,20,23,24	74 F2[illegible]3
IC21	74 F32
IC25	74 S74
IC27	32 x 8 PROM
IC28,34	74 S04
IC31	74 F374
IC33	74LS298
D1	1N914
TR1	2N2369

RESISTORS

R1,2,3,4,5 7,11,12	2K2
R6	1K0
R8,9,10	22R
RP1	4K7 x 8 S.I.L.

CAPACITORS

C1,2	22u Tant.
C3,4,5,6,7,8 9,10,11,15,16 17,18,19,20 21,22,23,24 25,26,27,28 29,30,31,32 33,34,35	0u22 Decoup.
C12,13	0u1 Ceramic
C14	4u7 Tant.
TC1	60p Trimmer

MISCELLANEOUS

DL1 226cm of tightly twisted, doubled wire on RM6 bobbin

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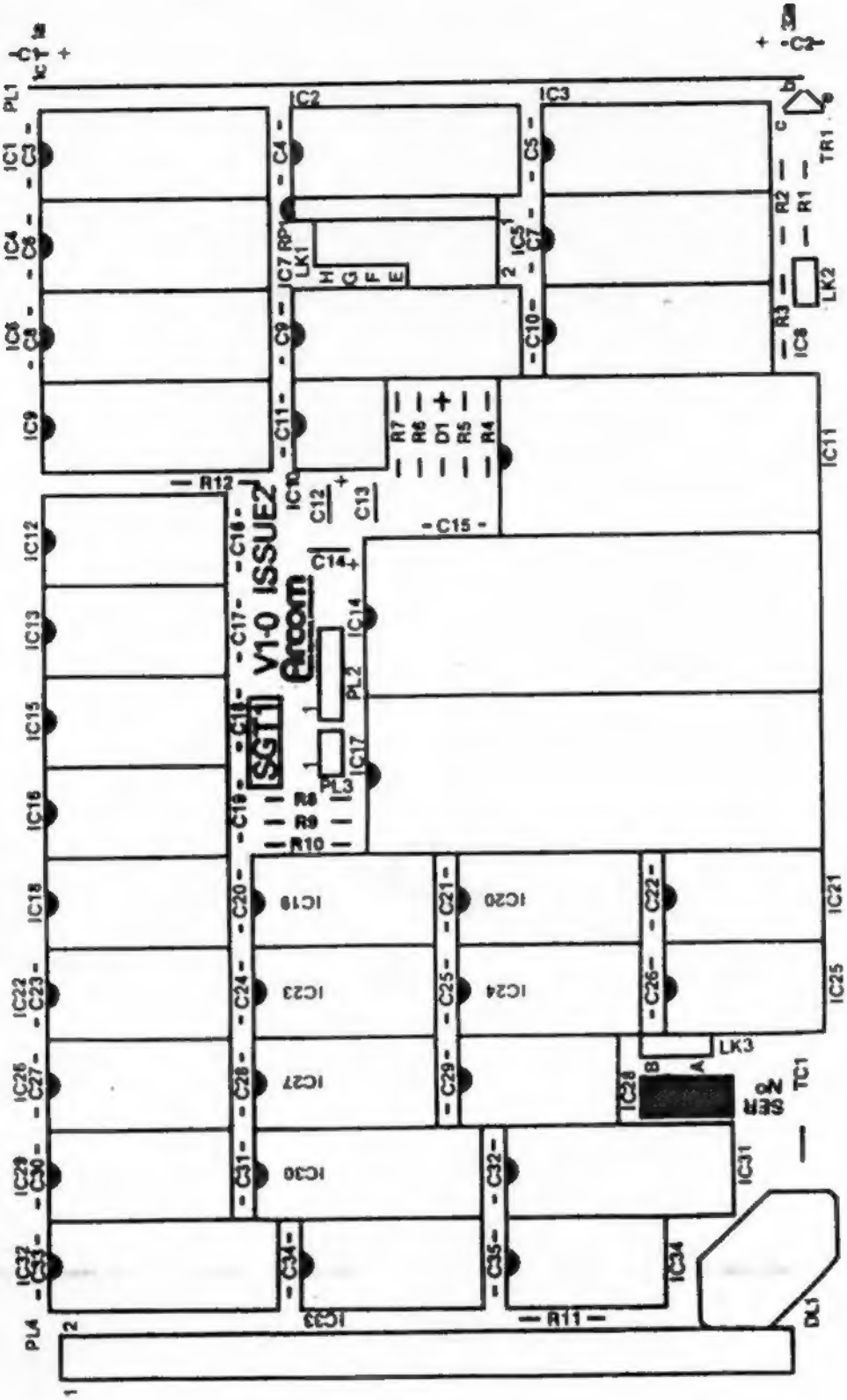

Version 1 Issue 2 Hardware

This version of the hardware will send a *DATACK back to the host processor about 10.5 us after a data write access.

Boards such as the Arcom SC09 require a *DATACK within 8us and so are not compatible with this version of the board.

A solution to this problem has been found and will be implemented on the version 1 issue 3 boards. Users who wish to use the SGT1 with a processor such as the SC09 should contact Peter Bhagat at Arcom.

With the majority of STEbus processor boards, including Arcom's SCPUA, SCPUB and SC88, this problem will not occur.